Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	1	(distribution adj unit) and (level adj fixing adj unit)	USPAT; USOCR; EPO; JPO; DERWENT	OR	OFF	2004/12/11 10:39
L2	2	(level adj fix$3) and (activation adj unit)	USPAT; USOCR; EPO; JPO; DERWENT	OR	OFF	2004/12/11 10:40
L3	285	test and (activation adj unit)	USPAT; USOCR; EPO; JPO; DERWENT	OR	OFF	2004/12/11 10:40
L4	0	3 and (level adj fixing)	USPAT; USOCR; EPO; JPO; DERWENT	OR	OFF	2004/12/11 10:40
L5	0	3 and SDRAM	USPAT; USOCR; EPO; JPO; DERWENT	OR	OFF	2004/12/11 10:40
L6	0	3 and DDR	USPAT; USOCR; EPO; JPO; DERWENT	OR	OFF	2004/12/11 10:41
L7	16	3 and DRAM	USPAT; USOCR; EPO; JPO; DERWENT	OR	OFF	2004/12/11 10:42
L8	8	3 and (distribution adj unit)	USPAT; USOCR; EPO; JPO; DERWENT	OR	OFF	2004/12/11 10:42
L9	6	3 and (input adj pin)	USPAT; USOCR; EPO; JPO; DERWENT	OR	OFF	2004/12/11 10:43
L10	53	3 and clock	USPAT; USOCR; EPO; JPO; DERWENT	OR	OFF	2004/12/11 10:43
L11	33	10 and address	USPAT; USOCR; EPO; JPO; DERWENT	OR	OFF	2004/12/11 10:45
L12	27	10 and (control adj signal)	USPAT; USOCR; EPO; JPO; DERWENT	OR	OFF	2004/12/11 10:46

L13	36	3 and (control adj signal)	USPAT; USOCR; EPO; JPO; DERWENT	OR	OFF	2004/12/11 10:47
L14	2	3 and (internal adj circuit)	USPAT; USOCR; EPO; JPO; DERWENT	OR	OFF	2004/12/11 10:47